PATENT ABSTRACTS OF JAPAN

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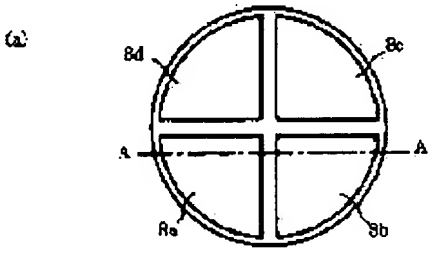
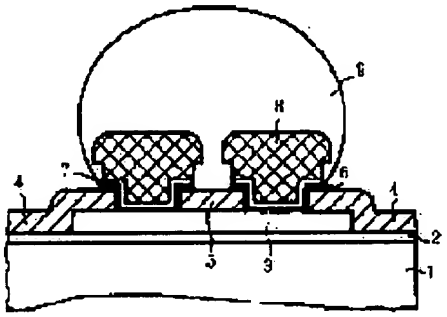
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:
PURPOSE: To prevent the generation of cracks by application of internal stress to the final insulating film on the overlapped part of a Cu plated layer, which constitutes a bump, and the final insulating film.
CONSTITUTION: A second insulating film 5 is formed on the aperture part of the final insulating film 4 located on the bonding part 3 provided through the intermediary of a first insulating film 2 on a semiconductor substrate 1, a plurality of bump-forming parts of the prescribed size are formed. On these divided parts, Cu-plated layers 8 are formed on the respective divided parts through the intermediary of a Cr layer 6 and a Cu layer 7, and a solder layer 9 is formed covering the Cu-plated layers 8 entirely. Accordingly, the stress added to the overlapped part of the individual Cu-plated layer and the final insulating film becomes very small by dividing the bump part, and as a result, the generation of cracks on the final insulating film can be prevented.





LEGAL STATUS
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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the semiconductor device which improved the structure of the bump section of a semiconductor device, and its manufacture method about a semiconductor device.
[0002]
[Description of the Prior Art] Sufficient adhesion edge to prepare a salient electrode (bump) in the conventional wirebonding method which pastes up between the electrode of a semiconductor device and the lead wire to the exterior on the point which should be mutually connected as a method of connecting electrically using narrow lead wire, and the electrode terminal of a semiconductor device, and paste up directly is formed, and the wireless-bonding method which connects with this bump simultaneously is indicated by JP,47-3206,B.
[0003] Drawing 8 (a) and (b) are the cross sections of the semiconductor device equivalent to the plan showing the electrode section of this conventional kind of semiconductor device, and its E-E line. The 1st insulator layer by which 1 was formed in the silicon substrate and 2 was formed on this silicon substrate 1 in this drawing, aluminum bonding pad used as the ground metal for 3 forming a bump, The last insulator layer from which 4 protects the aforementioned aluminum bonding pad 3 and aluminum wiring (not shown) (GARASUKO-TO film), It is Cr layer by which 6 was formed on the aforementioned aluminum bonding pad 3, Cu layer by which 7 was formed on this Cr layer 6, Cu deposit by which 8 was formed of electroplating on this Cu layer 7, and the solder layer by which 9 was formed on this Cu deposit 8, and the bump is formed on these each class.
[0004] The conventional semiconductor device is constituted as mentioned above. the 1st insulator layer 2 About 0.7 micrometers is deposited on a silicon substrate 1 by SiO2 film which includes several mol % of Lynn with reduced pressure CVD, and the aluminum bonding pad 3 is what deposited about 1 micrometer of thickness in the sputtering system. It is SiO2 which it is a ground metal for forming a bump, and the last insulator layer 4 is for protecting the aforementioned aluminum wiring and the aluminum bonding pad 3, and includes Lynn. SiO2 which does not include a film and Lynn SiO2 by CVD of membranous two-layer structure Generally the film is used. In order that the Cr layer 6 and the Cu layer 7 may lessen the impurities (O2 etc.) of a Cr-Cu interface, it has deposited continuously in the same sputtering system, and the Cr layer 6 is what was deposited about 0.1 micrometers of thickness. It is for strengthening adhesion of the aluminum bonding pad 3 and the Cu layer 7, and the Cu layer 7 is what was deposited several micrometers thickness. Becoming an electrode at the time of forming the Cu deposit 8 with electrolysis plating (cathode), since wettability with the solder layer 9 is good, it is used, and the Cu deposit 8 is 10 micrometers of thickness numbers, and pastes up the solder layer 9 by the printed circuit board and face down bonding. The diameter of a bump is about 200 micrometers, and a bump's height is several micrometers.
[0005] Next, the conventional bump formation process is explained about drawing 9 and drawing 10 . At drawing 9 (a), it is SiO2 of about 0.7 micrometers of thickness by reduced pressure CVD as the 1st insulator layer 2. After carrying out the depository of the film, The aluminum bonding pad 3 is formed in about 1-micrometer thickness by the sputtering system. Furthermore, what formed the last insulator

layer 4 by CVD on it is shown, and the ****** back of the portion which forms a bump by photoengraving process at drawing 9 (b) is shown. in drawing 9 (c) It is shown after depositing the Cr layer 6 of about 0.1 micrometers of thickness, and the Cu layer 7 of about 1.0 micrometers of thickness all over a wafer in a sputtering system. in drawing 10 (a) Except the bump formation section, it covers by the resist 10 and electrolysis plating shows the formation back of the Cu deposit 8 of about 15 micrometers of thickness to the bump formation section. in drawing 10 (b) The etching back of the Cr layer 6 and the Cu layer 7 is shown after removing a resist 10, by drawing 10 (c), the solder layer 9 is formed on the Cu deposit 8, and the completion back of bump formation is shown.

[0006]

[Problem(s) to be Solved by the Invention] With a semiconductor device with the conventional bump structure formed as mentioned above, when forming the Cu deposit 8, in the portion which overlaps the Cu deposit 8 and the last insulator layer 4, internal stress joined the last insulator layer 4, and there was a trouble that a crack 11 occurred like drawing 11 .

[0007] As mentioned above, in order to solve the mechanism by which a crack 11 goes into the last insulator layer 4 in the portion which overlaps the Cu deposit 8 and the last insulator layer 4, artificers investigated the relation between the diameter of a bump, and the rate of crack initiation of the last insulator layer 4 about the cause of generating that a crack 11 enters. The relation between this diameter of a bump and the rate of crack initiation of the last insulator layer 4 is shown in drawing 12 .

[0008] When the diameter of a bump was enlarged so that drawing 12 might show, the incidence rate of a crack 11 became high, less than [phi100micrometer], the rate of crack initiation is very small, and the bird clapper found the diameter of a bump.

[0009] In a semiconductor device, the mechanism by which a crack 11 goes into the last insulator layer 4 is considered as follows. That is, when forming the Cu deposit 8 with electrolysis plating, Cu atom in copper-sulfate liquid moves to a bump formation portion, and the Cu deposit 8 is formed. Under the present circumstances, it is for the shrinkage force of the Cu deposit 8 accompanying movement of Cu atom to join the last insulator layer 4 of the formation section circumference of the Cu deposit 8, and it is thought that the contraction is proportional to the diameter of a bump.

[0010] this invention was not made in order to cancel the above troubles, and it aims at acquiring the semiconductor device with which a crack does not go into the last insulator layer, and its manufacture method.

[0011]

[Means for Solving the Problem] The semiconductor device according to claim 1 concerning this invention divides the interior of a bump on a bonding pad into the necessary configuration of the size below predetermined.

[0012] Moreover, the manufacture method of a semiconductor device according to claim 2 forms an insulator layer on a semiconductor substrate, forms a bonding pad on it, forms the insulator layer for dividing a bump on this bonding pad, continues and forms Cr layer and Cu layer on this, forms Cu deposit and a solder layer on it further, and forms a bump.

[0013]

[Function] In the claim 1 of this invention, by having divided the interior of a bump, the internal stress which joins the last insulator layer is eased, and generating of a crack is suppressed.

[0014] Moreover, in a claim 2, since form the last insulator layer on the bonding pad on a semiconductor substrate, the 2nd insulator layer is formed so that a bump may be divided on the opening, Cu deposit is formed in each of the division portion and a bump is formed, where Cu deposit formed on a bonding pad is divided, it is formed inside a bump.

[0015]

[Example] Hereafter, one example of this invention is explained based on a drawing. Drawing 1 (a) and (b) are the cross sections of the semiconductor device equivalent to the plan except the solder layer and its A-A line of electrode section of this invention. [of a semiconductor device] it is shown in drawing 1 -- as -- 1-4 -- the above -- it is completely conventionally the same as that of equipment 5 makes the interior of a bump quadrisection on the aluminum bonding pad 3 which is a ground metal for forming a bump. The 2nd insulator layer of 40 micrometers of **** for setting the size of each division

portion to about 100 micrometers or less, Cr layer by which 6 was formed on the 2nd insulator layer 5 and the last insulator layer 4 with the aforementioned aluminum bonding pad 3 top and about about 5-micrometer overlap portion, 7 is Cu layer formed on this Cr layer 6, 8 (8a-8d) is Cu deposit each grew up to be in the quadrisection portion, and 9 is the solder layer formed on this Cu deposit 8.
[0016] Next, the bump formation process of drawing 1 is explained about drawing 2 , drawing 3, and drawing 4 . Drawing 2 (a) is SiO2 of about 0.7 micrometers of thickness as the 1st insulator layer 2 like drawing 9 (a). After carrying out the depository of the film, the state where the aluminum bonding pad 3 and the last insulator layer 4 were formed is shown, and drawing 2 (b) carries out patterning of the last insulator layer 4. Internal division of the portion which forms a bump in the opening by photoengraving process is carried out by forming the 2nd insulator layer 5 of 35 micrometers of ****. The state where the size of each division portion was set to about 100 micrometers or less is shown. drawing 2 (c) It is shown after depositing the Cr layer 6 of about 0.1 micrometers of thickness, and the Cu layer 7 of about 1.0 micrometers of thickness continuously in a sputtering system, and drawing 3 (a) shows, after covering by the resist 108 so that the Cr layer 6 and the Cu layer 7 may be exposed to the portion by which the interior which forms a bump was quadrisected. Moreover, drawing 3 (b) shows, after forming the Cu deposit 8 (8a-8d) of about 15 micrometers of thickness by electrolysis plating. As for drawing 3 (c), drawing 4 (a) after resist removal shows the state where the Cu layer 7 formed in the mask by the spatter in the Cu deposit 8 was further removed by etching. Furthermore, drawing 4 (b) is immersed in a solder tub in a wafer, and shows the state where formed the solder layer 9 and the bump was formed on the Cu deposit 8.
[0017] In the semiconductor device constituted as mentioned above By quadrisecting the interior of a bump by the 2nd insulator layer 5, and setting the size of each division portion to about 100 micrometers or less Since the Cu deposit 8 of the quadrisected portion grows without contacting mutually in case the Cu deposit 8 grows, the stress which joins the last insulator layer 4 can be stopped very low compared with the conventional structure, therefore generating of the crack 11 of the last insulator layer 4 can be prevented.
[0018] In addition, although the interior of a bump is quadrisected and the size of each division portion is set to about 100 micrometers or less in the example of above-mentioned drawing 1 , the effect same as for small division (for example, eight division, 16 division, etc.) is expectable in this example to set the size of the division portion inside a bump to about 100 micrometers or less.
[0019] Drawing 5 (a), and (b) are drawings showing the example which carried out the interior of a bump comparatively for 8 minutes, are the same drawing as drawing 1 (a), and (b), and drawing 6 (a), and (b) are the examples which show the structure which carried out the array partitioning of the polygons, such as a hexagon, to roughness and fineness, drawing 7 (a), and (b) are drawings showing the structure which carried out an array partitioning to the shape of a doughnut, and they In addition, drawing 5 (b), drawing 6 (b), and drawing 7 (b) are the cross sections of the semiconductor device which is equivalent to drawing 5 (a), drawing 6 (a), the B-B line of drawing 7 (a), a C-C line, and D-D line, respectively.
[0020]
[Effect of the Invention] As explained above, since the semiconductor device according to claim 1 by this invention divides Cu deposit and forms the division portion in about 100 micrometers or less, respectively, it eases the internal stress to the last insulator layer by Cu deposit, and has the effect which suppresses generating of a crack.
[0021] Moreover, the manufacture method of a semiconductor device according to claim 2 So that the 2nd insulator layer may be formed in opening of the last insulator layer by which opening was carried out and the bump of a predetermined size may be formed on the bonding pad on a semiconductor substrate in a necessary configuration And since it divides into a required number and Cu deposit is formed in each of these division portions, a solder layer is formed and a bump is formed so that the whole Cu deposit divided and formed may be covered The internal stress to the last insulator layer by each Cu deposit becomes very small, and can prevent generating of the crack to the last insulator layer.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the important section of the semiconductor device which is one example of this invention.
[Drawing 2] It is the cross section showing the formation process of the bump of this invention.
[Drawing 3] It is the cross section showing the process which follows drawing 2 .
[Drawing 4] It is the cross section showing the process which follows drawing 3 .
[Drawing 5] It is drawing showing the important section of other examples of this invention.
[Drawing 6] It is drawing showing the important section of the example of further others of this invention.
[Drawing 7] It is drawing showing the important section of the example of further others of this invention.
[Drawing 8] It is drawing showing the important section of the conventional semiconductor device.
[Drawing 9] It is the cross section showing the conventional manufacturing process.
[Drawing 10] It is the cross section showing the process which follows drawing 8 .
[Drawing 11] It is the cross section showing the trouble of the conventional semiconductor device.
[Drawing 12] It is drawing showing the relation between the diameter of a bump, and the rate of crack initiation to the last insulator layer.
[Description of Notations]
1 Silicon Substrate
2 1st Insulator Layer
3 Aluminum Bonding Pad
4 The Last Insulator Layer
5 2nd Insulator Layer
6 Cr Layer
7 Cu Layer
8 Cu Deposit
9 Solder Layer
10 Resist

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* NOTICES *

CLAIMS

[Claim(s)]

[Claim 1] The semiconductor device characterized by dividing the aforementioned interior of a bump into the necessary configuration of the size below predetermined in the semiconductor device with which the bump was formed in opening of the last insulator layer on the bonding pad prepared through the 1st insulator layer on the semiconductor substrate.

[Claim 2] The manufacture method of a semiconductor device characterized by providing the following. The process which forms the 2nd insulator layer for dividing a bump into opening of the last insulator layer which formed the bonding pad on the 1st insulator layer of a semiconductor substrate, and was formed on this bonding pad. The process which forms Cr layer and Cu layer for forming a bump on the aforementioned bonding pad by the continuation spatter. The resist process which exposes Cr layer and Cu layer to the division portion of the bump formation section. The process which forms Cu deposit in a division portion, the ESSHINGU process which removes a spatter Cr layer and a spatter Cu layer for this Cu deposit on a mask, and the process which forms a solder layer on the aforementioned Cu deposit.

[Translation done.]